1 0

1.4 2024.4

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1

1.1

1.2

1.3

1.4

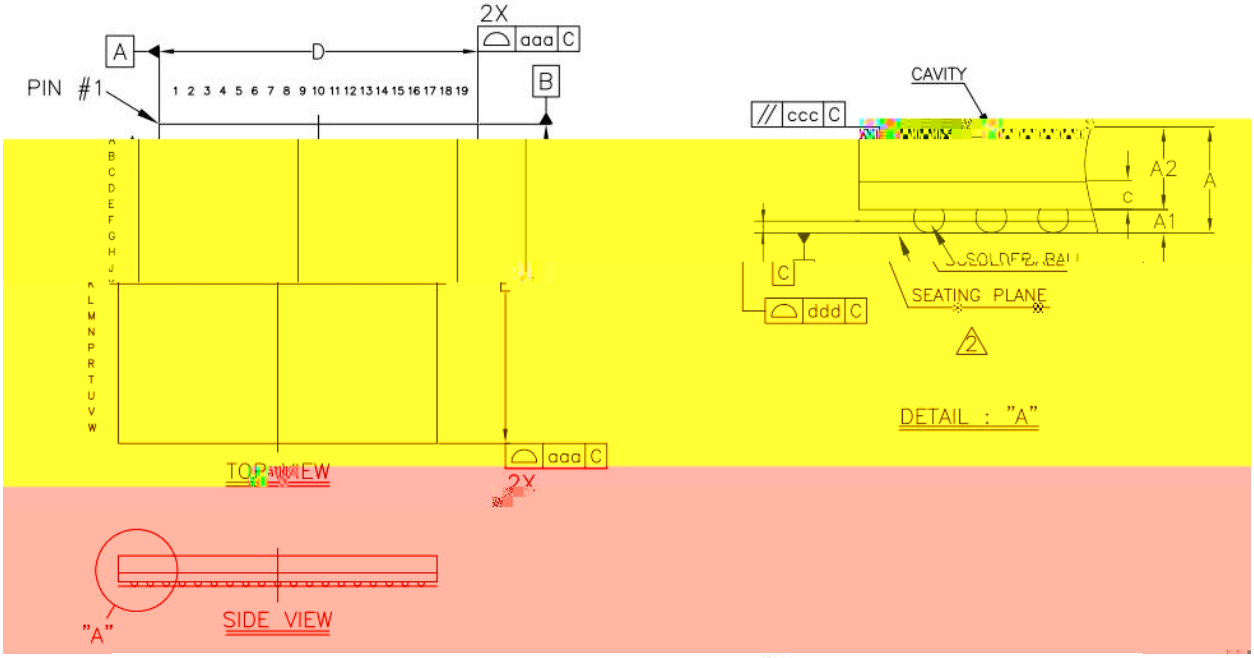
1.5

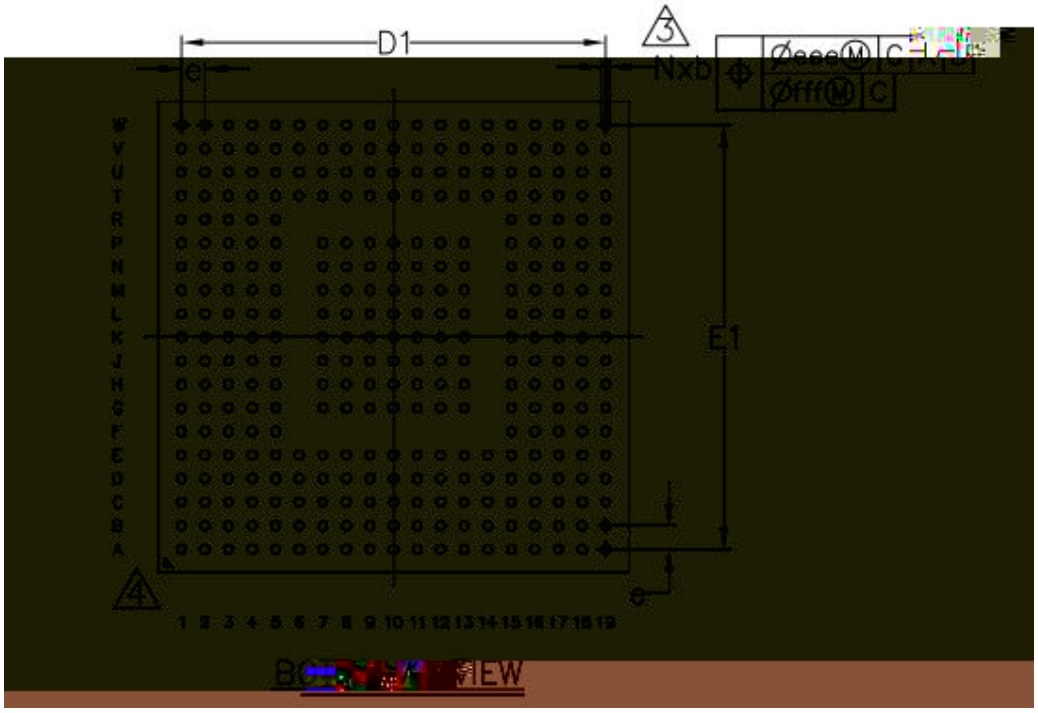
1.

1.

2

2.1


2X
aaa C
A
D
B
PIN #1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
A B C D E F G H J K L M N P R T U V W
E
aaa C
2X
TOP VIEW
"A"
SIDE VIEW
CAVITY
// ccc C
A2
A
c
A1
C
ddd C
SEATING PLANE
2
DETAIL : "A"


D1
e
3
Nxb
Øeee M C
Øfff M C
W V U T R P N M L K J H G F E D C B A
E1
4
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
e
BOTTOM VIEW

2.2

2.3

2.3.1

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2.3.2 #0

2.3.4 #1

2.3.5 #1

2.3.

2.3. #3 (4-)

2.3.10

2.3.11

2.3.12 15

2.3.13

2.3.14

2.3.15

2.3.1

2.3.1

2.4

3

3.1

	-65		140	°C
Tj(PN)	-55		125	°C
VCCK VCC11A	-0.1	1.1	1.155	V
VCC11A_PE,VCC11A_A10,VCC11A_CEN,VCC11A_PLL	-0.1	1.1	1.155	V
VCC3IO,VCC33A VCC33	-0.4	3.3	3.7	V
VCC18IO_25V	-0.4	3.3	3.7	V

3.2

	-40		85	°C
VCCK VCC11A	1.045	1.1	1.155	V
VCC11A_PE,VCC11A_A10,VCC11A_CEN,VCC11A_PLL	1.045	1.1	1.155	V
VCC3IO,VCC33A VCC33	3.135	3.3	3.465	V
VCC18IO_25V	3.135	3.3	3.465	V

3.3

IO reference voltage	Vref		3.0	3.3	3.6	V
Input low voltage	Vil				0.8	V
Input high voltage	Vih		2.0			V
Input low current	Iil	Vin=0V	-20		0	μA
Input high current	Iih	Vin=Vref-Vref,max	0		200	μA
Output low voltage	Vol	Iol=4mA,Vref=min	0		400	mV
Output high voltage	Voh	IOh=-4mA,Vref=min	2.4		Vref	V

3.4

Tckf	NCSI_REF_CLK Frequency		50		MHz
Rdc	NCSI_REF_CLK duty cycle	35		65	%
Racc	NCSI_REF_CLK accuracy			100	ppm
Tco	Clock-to-out (10 pF =< cload <=50 pF) NCSI_RXD[1:0], NCSI_CSR_DV Data valid from NCSI_REF_CLK rising edge	2.5		12.5	ns
Tsu	NCSI_TXD[1:0], NCSI_TX_EN Data Setup to NCSI_CLK_IN rising edge	3			ns
Thold	NCSI_TXD[1:0], NCSI_TX_EN Data hold from NCSI_REF_CLK rising edge	1			ns
Tor	NCSI_RXD[1:0], NCSI_CSR_DV Output Time rise	0.5		6	ns
Tof	NCSI_RXD[1:0], NCSI_CSR_DV Output Time fall	0.5		6	ns
Tckr/Tckf	NCSI_REF_CLK Rise/Fall Time	0.5		3.5	ns

3.5

Frequency	-	-	25	-	MHz

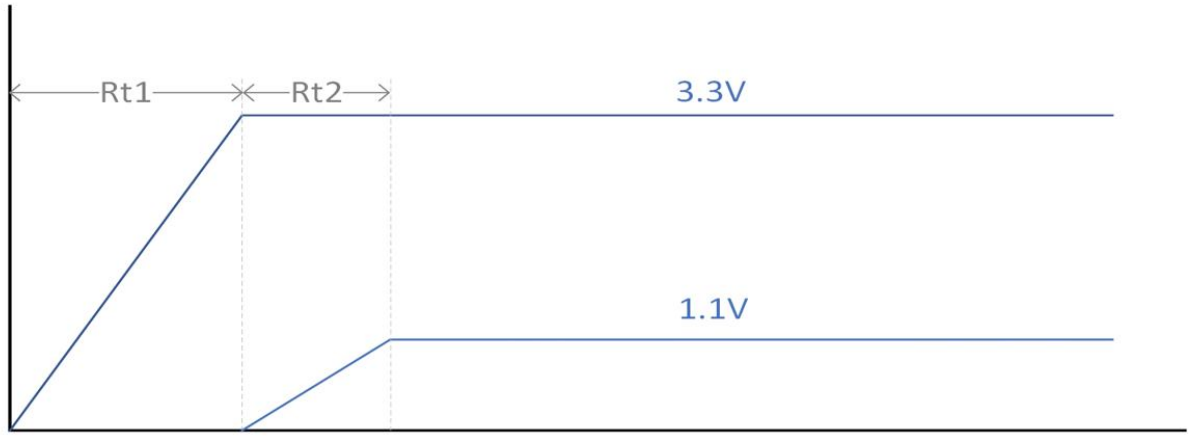
Vibration mode			Fundamental		
Frequency Stability	Ta=0-70	-30		+30	ppm
Frequency Tolerance	Ta=25	-50		+50	ppm
Load Capacitance			20		pf

Frequency	-	-	25	-	MHz
Frequency Stability	Ta=0-70	-30		+30	ppm
Frequency Tolerance	Ta=25	-50		+50	ppm
Duty Cycle		40		60	%
Broadband Peak-to-peak Jitter				200	ps
Vpeak-to-peak		3.135	3.3	3.465	V
Rise time 10%-90%				10	ns
Fall time 10%-90%				10	ns
Operation temperature Range		0		70	

3.5

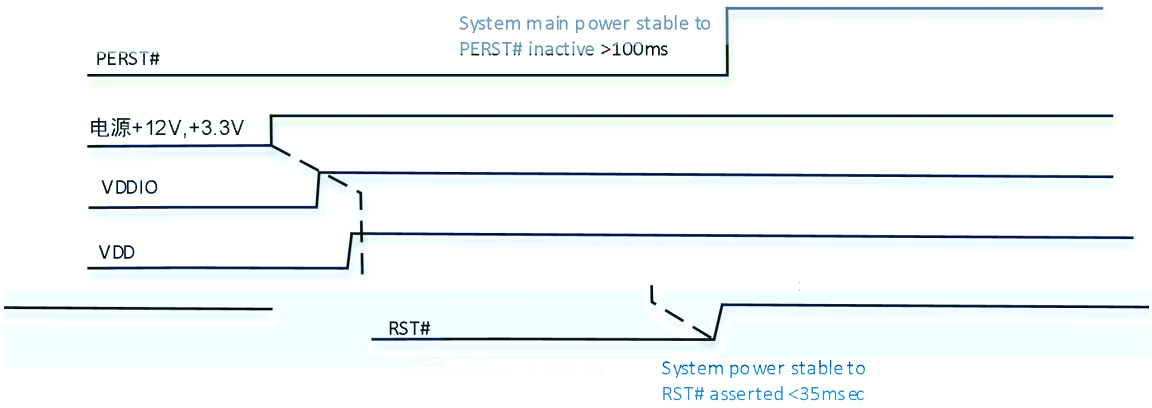
GPHY IP 1.1V 3.3V 5ms 3.3V rise time 1ms

3.3V 1.1V



Rt1	3.3V rise time	1	-	100	ms
Rt2	3.3V ready to 1.1V ready time	-5	-	-	ms

WX1860 RST# J1 PERST# G3



VDDIO VCCIO VCC33A VDD VCCK VCC11A

3.6

WX1860 socket socket Z390-A PCI
4 CH1 CH2 CH3 CH4
1000M WX1860A4/WX1860AL4 70

4

winbond	W25Q80DV
microchip	SST25VF080B
	GD25Q80

5

1	WX1860A2		0 -70 ,40nm,2	2
2	WX1860A4		0 -70 ,40nm,4	4
3	WX1860AL1		-40 -85 ,40nm,1 SM2/SM3/SM4	1
4	WX1860AL2		-40 -85 ,40nm,2 SM2/SM3/SM4	2
5	WX1860AL4		-40 -85 ,40nm,4 SM2/SM3/SM4	4

1 N0 2 N0 N1 N2 N3
N0 N1 N2 N3